REMARKS

Claims 1-30 have been examined and are now pending in the application. Reexamination and reconsideration of all outstanding rejections and objections are requested.

Claims 1-30 are rejected under 35 U.S.C. §102(e) as being anticipated by Hayter et al.

Claim 1 recites an interface for a network device and a CPU, with the interface including a shared memory including a Rx buffer pool, maintained in the shared memory and which is write-only by the CPU and read-only by the device, comprising a plurality of buffer pool entries, each entry holding an address and length value of a scatter-gather buffer; a transmit FIFO pool which is write-only by the CPU and read-only by the device, with each FIFO pool entry holding a buffer length, start field, end field, and buffer address field; a status ring, maintained in shared memory and which is read-only by the CPU and write-only by the device, with each status ring entry holding status information written by the device and a toggle bit which holds a value which is changed by the device each time the device accesses the status ring; and a private memory, accessible only by the CPU, with the private memory holding a shadow copy of the scatter/gather buffers, in software-friendly form, included in the received buffer pool and a shadow count of the number of available of Tx FIFO entries.

The reference Hayter discloses a system for packet processing. In Hayter a device, i.e., the Packet Interface Circuit, DMA's (writes) the packet data into memory through the I/O bridge and memory controller. [0027] The DMA utilizes descriptor's to write received data into receive buffers in the shared memory. [0031]. The DMA controller of the device also writes data to the Tx FIFO. [0031]

The basic requirements for anticipation are set forth in MPEP §2131: A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

The recited shared memory including an Rx buffer pool which is read-only by the device is not found in Hayter. As described above, the Packet Interface Circuit DMA's (writes) data into the Rx buffers. Accordingly, the element of an Rx buffer pool that is read only by the device is not found in the reference.

The recited transmit buffer pool that is read-only by the device is not found in Hayter. As described above, the DMA controller of the Packet Interface Device writes data to the Tx FIFOs. Accordingly, the element of a transmit FIFO which is read-only by the device is not found in the reference.

The recited private memory, accessible only by the CPU, with the private memory holding a shadow copy of the scatter/gather buffers, in software-friendly form, included in the received buffer pool and a shadow count of the number of available of Tx FIFO entries is not found in Hayter. All the citations in the office action refer to either the L2 cache 14 or Memory 28. Neither of these structures include the private memory recited in claim 1.

The interface described in Hayter is the same as the conventional interface depicted in Fig. 1 of the present application and described at paragraphs [42]-[43].

Independent claims 3, 4, 6, 7, 9, 10, 11, 12, and 13 recite similar limitations as claim 1 and are allowable for the same reasons. Claims 2, 5, 8 are dependent claims which are allowable for the same reasons as the independent claims from which they depend.

Claim 14 recites a method for fairly allocating receive buffers in an interface between a plurality of line cards and a CPU, where interface includes a like plurality of budget counters holding LC budget value, each associated with a particular line card, and a receive buffer counter holding a receive buffer value indicating a number of available receive buffers for holding packets received at the line card. The method comprises the following steps implemented at the CPU. Initializing each LC budget value to a ratio of the bandwidth of the line card associated with the budget counter to the total bandwidth of all line cards coupled to the interface, scaled to a number of receive interface buffer resources available to the interface; incrementing the LC budget value associated with a particular line card when the CPU processes a receive buffer holding packet data stored by the particular line card; incrementing the receive buffer when the CPU processes a receive buffer holding packet data; decrementing the LC budget value associated with a particular line card when the interface receives packet data from the line card and places the packet data in a receive buffer; decrementing the receive buffer when the interface receives packet data from a line card and places the packet data in a receive buffer; and dropping packets from a line card when the associated LC budget value is zero or less.

There is no teaching in Hayter of a plurality of budget counters having LC budget values initialized, incremented, and decremented as recited in claim 14.

Referring to the citations in the office action, paragraph [30] discloses FIFOs for holding Tx and Rx data, paragraph [23] describes Fig. 1 which shows no budget counters, paragraph [82] describes the transfer of a cache block by the DMA, there is no teaching relating to the claimed steps, paragraph [64] describes the assertion of a L2 cache signal, and paragraph [86] describes the DMA updating a configuration register to indicate the next unused descriptor. The subject matter recited in claim 14 is not found in any of these citations.

Claims 15 and 16 recite limitations similar to claim 14 and are allowable for the same reasons.

Claim 17 recites a system for transferring transmit packet data to a transmit interface, that comprises a processor module including a processor and a data mover, with the data mover having access to the module internal resources; a memory holding a transmit ring and buffers, with each transmit ring entry for holding an address of a transmit buffer, and with the memory holding a data mover descriptor ring which is initialized by the processor; a high-speed bus coupled to the memory and the processor module; an interface module coupling the high-speed bus to the transmit interface, with the interface module responding to a transmit indication to read a transmit ring entry from the memory, to translate a transmit ring entry into a data mover descriptor, to write a translated data mover descriptor to the data mover descriptor ring for each transmit ring entry of a packet to be transmitted, to write a terminator descriptor to the data mover descriptor ring when the end of the packet is detected, and then to signal the data mover to read the data mover descriptors from the data mover descriptor ring; and with the data mover initiating packet data transfer to the interface module when signaled by the interface module.

The claimed interface module the with the interface module responding to a transmit indication to read a transmit ring entry from the memory, to translate a transmit ring entry into a data mover descriptor, to write a translated data mover descriptor to the data mover descriptor ring for each transmit ring entry of a packet to be transmitted, to write a terminator descriptor to the data mover descriptor ring when the end of the packet is detected is not found in Hayter.

Referring to the citations in the office action, Fig. 1 depicts a standard packet processing system that does not include a data mover or a translation mechanism, Fig. 3 depicts how the packet interface circuit stores a header in the L2 cache and data in shared memory, paragraph [75] describes the buffer descriptors, paragraph [31] describes how the DMA utilizes descriptors to move data, paragraph [34] describes how data is transferred to the Tx FIFO, and paragraph [48] describes general memory transactions. None of limitations in claim 17 described above are found in the citations.

Claims 18, 20, 22 are independent claims that recite limitations similar to those described above in claim 17. Accordingly, those claims are allowable for the same reasons as claim 17. Claims 19, 21, and 23 are dependent claims allowable for the same reasons as the claims from which they depend.

Claim 25 recites a method for implementing packet transmit flow control in a system including a processor, memory, and interface module, coupled by a high-speed bus, with the interface module able to directly access processor memory and interfacing the high-speed bus with transmit interfaces, and with memory holding an xon/xoff table and an xon status ring initialized by the processor, said method comprising the steps of: at the interface module, maintaining the xon/xoff table to indicate the current xon/xoff transmit status of the transmit interfaces, writing an entry to the xon status ring indicating an interface that transitions from xoff to xon, and interrupting the processor subsequent to writing to the xon status ring; and at the processor, responding to the interrupt to read the xon entry, checking whether packets are holding to transmit over the identified interface, and indicating to the interface module when the xon status ring entry has been processed.

The claimed maintaining an xon/xoff table at an interface module, writing an entry to the xon status ring indicating an interface that transitions from xoff to xon, and interrupting the processor subsequent to writing to the xon status ring; and at the processor, responding to the interrupt to read the xon entry, checking whether packets are holding to transmit over the identified interface, and indicating to the interface module when the xon status ring entry has been processed are not found in Hayter.

There is no disclosure of an xon/xoff table in Hayter or of the claimed steps.

Independent claims 24, 27 and 29 recite limitations similar to those described above in claim 24 and are allowable for the same reasons. Dependent claims 26, 28, and 30 are allowable for the same reasons as the claims from which they depend.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 944-3320.

Respectfully submitted,

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